IN THE CLAIMS:

Claims 1 and 15 have been amended herein. All of the pending claims 1 through 15 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Currently Amended) A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, said semiconductor substrate including at least one opening extending therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; and

at least one piece ~~two pieces~~ of adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of the one piece ~~of the two pieces~~ of adhesive tape extending at least one of beyond said edge of said at least one semiconductor substrate opening a distance into said at least one semiconductor substrate opening to provide a detectable surface within said at least one semiconductor substrate opening and beyond said edge of said at least one semiconductor die a distance on said semiconductor substrate first surface to provide a detectable adhesive tape surface on said semiconductor substrate first surface ~~proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening, a width of another piece of the two pieces of adhesive tape extending at least proximate another edge of said at least one semiconductor substrate opening, a contact area between said at least one semiconductor die and said semiconductor substrate being substantially maximized~~.

2. (Previously Presented) A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening, said electrical connection area disposed on said semiconductor die active surface, said at least one electrical connection area directly connected to at least one output electrical connection of said semiconductor device; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of said at least one adhesive tape extending at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening, said width of said at least one adhesive tape extends beyond said edge of said at least one semiconductor substrate opening a distance into said at least one semiconductor substrate opening to provide a detectable surface within said at least one semiconductor substrate opening.

3. (Previously Presented) A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening, said at least one electrical connection area disposed on said semiconductor die active surface, said at least one electrical connection area directly connected to at least one output electrical connection of said semiconductor device; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of said at least one adhesive tape extending at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening and extending beyond said edge of said at least one semiconductor die a distance on said semiconductor substrate first surface to provide a detectable adhesive tape surface on said semiconductor substrate first surface.

4. (Original) The semiconductor die assembly of claim 1, further including at least one electrical connection extending between said at least one electrical connection area and at least one trace on said semiconductor substrate second surface.

5. (Original) The semiconductor die assembly of claim 4, wherein said at least one electrical connection comprises a bond wire.

6. (Original) The semiconductor die assembly of claim 4, wherein said at least one electrical connection comprises a TAB connection.

7. (Original) The semiconductor die assembly of claim 4, further including a glob top material disposed within said at least one semiconductor substrate opening encasing said at least one electrical connection.

8. (Original) The semiconductor die assembly of claim 7, further including an encapsulant material encasing said at least one semiconductor die and said glob top material.

9. (Original) The semiconductor die assembly of claim 1, wherein said at least one adhesive tape comprises a planar carrier film including a first surface having a first adhesive disposed thereon and a second surface having a second adhesive disposed thereon.

10. (Previously Presented) A semiconductor die assembly comprising:
a semiconductor substrate having a first surface and a second surface, wherein said

semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; and

at least one adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of said at least one adhesive tape extends at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening, said at least one adhesive tape comprises a planar carrier film including a first surface having a first adhesive disposed thereon and a second surface having a second adhesive disposed thereon, and the composition of said first adhesive differs from a composition of said second adhesive for substantially preventing damage to a portion of the active surface of the semiconductor die by filler particles in a material used to fill the at least one opening in the substrate being located between the first surface of the substrate and the active surface of the at least one semiconductor die.

11. (Original) The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate said at least one adhesive tape and said edge of said at least one semiconductor die.

12. (Original) The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate said at least one adhesive tape and said edge of said at least one semiconductor substrate opening.

13. (Original) The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate said at least one adhesive tape and said active surface of said at least one semiconductor die.

14. (Original) The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate said at least one adhesive tape and said semiconductor substrate first surface.

15. (Currently Amended) A computer comprising:

at least one semiconductor die assembly, said semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein said semiconductor substrate includes at least one opening defined therethrough between said semiconductor substrate first surface and said semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on said semiconductor die active surface, said at least one semiconductor die oriented having said at least one electrical connection area substantially aligned with said at least one semiconductor substrate opening; and

at least one piece ~~two pieces~~ of adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of one piece of adhesive tape of the two pieces of adhesive tape extending at least one of beyond said edge of said at least one semiconductor substrate opening a distance into said at least one semiconductor substrate opening to provide a detectable surface within said at least one semiconductor substrate opening and beyond said edge of said at least one semiconductor die a distance on said semiconductor substrate first surface to provide a detectable adhesive tape surface on said semiconductor substrate first surface ~~proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening, a width of the other piece of adhesive tape of the two pieces of adhesive tape extending at least proximate an edge of said at least one semiconductor die to an opposite edge of said at least one semiconductor die, a contact area between said at least one semiconductor die and said semiconductor substrate being substantially maximized~~.